REMARKS/ARGUMENTS

Reconsideration of the present application, as amended, is respectfully requested.

The March 20, 2006 Office Action and the Examiner's comments have been carefully considered. In response, claims are amended and remarks are set forth below in a sincere effort to place the present application in form for allowance. The amendments are supported by the application as originally filed. Therefore, no new matter is added.

ABSTRACT OF THE DISCLOSURE

The Abstract of the Disclosure is amended to be in better form. No new matter is added and a replacement sheet of the Abstract of the Disclosure without bracketing, strike-outs and underlining is attached to this response.

PRIOR ART REJECTION

In the Office Action, claims 1-6 are rejected under 35 USC 102(b) as being anticipated by U.S. Patent Publication No. 2005/0030207 (Craven et al.).

In response, independent claims 1, 3 and 4 are amended to clarify the invention.

Claim 1 now recites a method of processing a signal using a digital signal processor having a given word length, the method including pre-processing the signal using a pre-processor which reduces the word length and performs an operation which is invariant with respect to a process being performed by the digital signal processor, transforming the pre-processed signal into frequency coefficients, and normalizing the frequency coefficients directly after the transformation of the pre-processed signal into frequency coefficients whereby quantization noise is thereby reduced in said process being performed by the digital signal processor.

A feature of the present claimed invention as defined by amended claim 1 is that after pre-processing of the signal, the pre-processed signal is transformed into frequency coefficients, e.g., by a Fast Fourier Transform (FFT) circuit and then directly thereafter, the frequency coefficients are normalized. This feature is described in the specification at, e.g., page 6, lines 3-6. By normalizing the frequency coefficients right after the FFT circuit, for example, by a symmetrical phase only matched filtering component (for example by element 13 in Fig. 3), quantization noise is reduced in the process being performed by the digital signal processor.

Claim 3, as amended, now recites a method of processing a signal received in the form of signal samples having a range of

sample values, the method including filtering the signal to reduce the range of signal sample values in a given band of non-interest, and thereafter digitally processing the filtered signal using integer arithmetic. Digital processing of the filtered signal includes transforming the filtered signal into frequency coefficients using an integer transform circuit.

Claim 4, as amended, now recites a digital signal processor including input means for receiving a signal in the form of integer signal samples having a range of sample values, filtering means for receiving the signal from the input means and reducing the range of signal sample values in a band of non-interest to form a filtered signal, and a digital signal processing circuit for receiving the filtered signal from the filtering means and digitally processing the filtered signal using integer arithmetic. The digital signal processing circuit includes an integer transform circuit that transforms the filtered signal into frequency coefficients.

As described in the specification at, e.g., page 7, lines 6-15, excessive quantization noise is obtained when an integer transform circuit, namely, an FFT circuit, is applied to an input signal to obtain a power spectrum representing an audio signal. However, this problem is overcome in the embodiments of the invention set forth in claims 3 and 4 by filtering the signal to reduce the range of signal sample values in a band of non-

interest. The filter signal can thus be digitally processed using integer arithmetic without resultant excessive quantization noise.

Craven et al. do not disclose, teach or suggest all of the features now set forth in the independent claims.

Craven et al. describe methods for encoding signals without losing data. One method entails "entropy coding" shortening as described in paragraph 155.

Craven et al. do not disclose transforming pre-processed signals into frequency coefficients, and normalizing the frequency coefficients directly thereafter, e.g., by means of a symmetrical phase only matched filtering unit which extracts the phase of the frequency coefficients. Craven et al. do not mention any normalization of transformed signals and therefore cannot anticipate or render obvious the embodiment of claim 1.

Craven et al. also do not disclose an integer transform circuit that transforms filtered signals into frequency coefficients (as opposed to digital signal processing using floating-point arithmetic). The Examiner referred to paragraph 176 to show use of integer arithmetic and referred to paragraph 191 to show use of a transform circuit, but no mention is made in either paragraph of the use of an integer transform circuit, e.g., an integer FFT circuit. As discussed above, particular problems with quantization noise arise from use of integer

transform circuits and the invention overcomes these particular problems by applying the filtering steps set forth in claims 3 and 4.

Since Craven et al. do not disclose an integer transform circuit, the disadvantages of such a circuit have not been appreciated by Craven et al. and therefore, the solution conceived by the inventors to address this problem, namely, pre-filtering the signal being processed to reduce the range of signal sample values in a band of interest, cannot be taught or suggested by Craven et al.

As such, Craven et al. cannot anticipate or render obvious the embodiments of claims 3 and 4.

In view of the foregoing, independent claims 1, 3 and 4 are patentable over Craven et al. under 35 USC 102 as well as 35 USC 103.

Claims 2, 5 and 6 are directly dependent on claim 1, claim 3 or claim 4 and are patentable over Craven et al. in view of their dependence on claim 1, claim 3 or claim 4 and because the references of record do not disclose, teach or suggest each of the limitations set forth in claims 2, 5 and 6.

In view of the foregoing, claims 1-6 are in form for immediate allowance, which action is earnestly solicited.

NEW CLAIMS

Claims 7-20 are presented. Claims 7-13 depend from claim 1 and set forth additional features of the signal processing method thereof which are described in the specification. Claims 14-18 depend directly or indirectly from claim 3 and set forth additional features of the signal processing method thereof which are described in the specification. Claims 19 and 20 depend directly or indirectly from claim 4 and set forth additional features of the digital signal processor thereof which are described in the specification. Claims 7-20 are patentable over the cited reference in view of their dependence on either claim 1, 3 or 4 and because the reference does not disclose, teach or suggest each of the limitations set forth in claims 7-20.

CLAIM FEE

No additional fee is due for the presentation of claims 7-20. However, if any additional fee is deemed to be due for entry of the Amendment, please charge Deposit Account No. 14-1270 for such sum.

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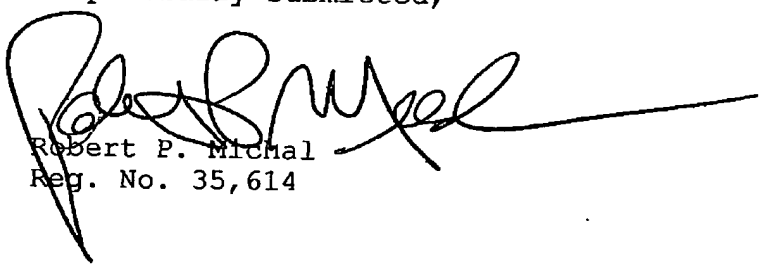
If the Examiner disagrees with any of the foregoing, the Examiner is respectfully requested to point out where there is support for a contrary view.

Entry of the amendment, allowance of the claims, and the passing of the application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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Encl.: Substitute Abstract of the Disclosure